

A condition monitoring method for solder layer degradation of liquid-cooled power semiconductors

Timm Felix Baumann^{1,2}, Konstantinos Papastergiou², Raul Murillo Garcia², Dimosthenis Peftitsis¹

¹ NTNU, Norway; ²CERN, Switzerland

Corresponding author: Timm Felix Baumann, timm.felix.baumann@cern.ch

D04 Stress Monitoring

Preferred presentation form: Oral presentation

Abstract

This paper presents a new method for condition monitoring of solder layer degradation of liquid-cooled power semiconductors. Solder layer degradation is detected by an increased thermal impedance, which has the effect that more heat is dissipated into the air instead of the cooling liquid. The proposed condition monitoring method is based on detecting the share of heat dissipated to the liquid and to the air. Experimental validation in a down-scaled laboratory setup is presented, with the focus for an application in an industrial converter.

1 Introduction

Condition monitoring of bond wires and solder layer in power semiconductor devices is crucial for optimised maintenance scheduling [1]. The most common condition monitoring method is based on monitoring the junction temperature. In most cases this temperature cannot be measured directly. It is possible to estimate the junction temperature by using the provided thermal model from the semiconductor manufacturer, case temperature and power dissipation. Still, solder layer delamination changes the thermal impedance, which must be taken into account for modeling the thermal network over time. Direct attachment of temperature sensors close to the dies has been shown as a method to measure the junction temperature [2] [3]. However, this necessitates complicated manufacturing due to space limitations. For this reason the junction temperature is estimated using temperature sensitive electrical parameters (TSEPs) [4]. However, TSEPs are also affected by degradation, thus necessitating re-calibration [5]. The degraded solder layer also affects the temperature distribution under the base plate. This can be detected by applying several temperature sensors under the base plate to monitor the heat spread [6]. Nevertheless, it is not practically feasible to place a large number of temperature sensors under each semiconductor device. This paper proposes a condition monitoring scheme for detecting solder delamination in liquid-cooled power semiconductors, without the need for junction temperature estimation. As solder delamination progresses, an increased amount of heat dissipation to the air instead through the base plate will occur. Thus, by monitoring the heat dissipated to the liquid and having the thermal network pre-characterized, solder layer degradation can be detected.

2 Proposed Condition Monitoring Scheme

To enable efficient loss heat dissipation, power semiconductors are mounted on a liquid cooling plate. The idea is to extract most of the dissipated power with the cooling liquid. Nevertheless, a fraction of this power will be dissipated into the air due to convection and thermal radiation. It is also possible that a percentage of the heat is exchanged between the liquid and air. In a practical converter, the air is often

forced, due to cooling requirements of auxiliary circuits. Therefore, the steady-state equivalent thermal network has a triangular form as shown in Fig. 1a.

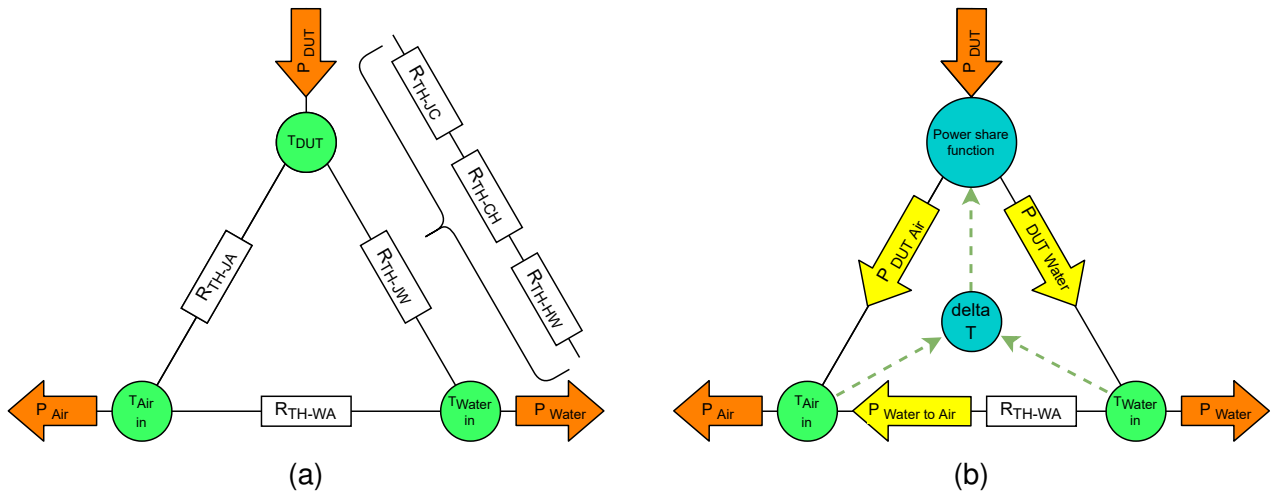


Fig. 1: Basic thermal network (a) and power share view (b)

In this thermal network, the junction temperature, T_{DUT} , temperature of the in-flowing liquid, $T_{water-in}$, and temperature of the incoming air, T_{air-in} are coupled by thermal impedances. Solder layer degradation means that the thermal impedance of the solder layer, R_{TH-JC} will increase. This internal thermal resistance is part of the thermal resistance to the liquid, R_{TH-JW} , together with the thermal resistance of the thermal connection, R_{TH-CH} and the heatsink, R_{TH-HW} (Fig. 1a). Therefore, an increase of R_{TH-JW} will change the thermal flow to the air and will increase the junction temperature. The share of the power that is dissipated into the water will indicate the state of health of the solder layer.

A key to apply the proposed method is the accurate estimation of the power dissipation from the semiconductors, as well as the accurate measurement of the power dissipated to the liquid. A detailed analysis on these issues will be included in the full paper.

2.1 Condition monitoring principle

With the given thermal network the power in the liquid can be estimated. The input of this model is the power dissipation (measured or calculated based on the mission profile). Additionally, the water inlet temperature and air inlet temperature must also be provided to the model as inputs. The flow rate of the liquid is part of the thermal impedances and should remain constant, which means that such measurement can be avoided in the field application. The condition monitoring principle is based on the comparison of the expected power dissipated in the water with the measured power in the water for a given load condition. If the percentage of the power dissipated into the liquid decreases, solder layer delamination is indicated. With the thermal model the current value of the thermal impedance R_{TH-JC} can be estimated.

2.2 Thermal model estimation

The thermal resistance defines the power flow depending on the temperature difference according to $R_{th} = \Delta T/P$. In this network, the thermal resistances cannot be estimated directly. A good approach is to perform a measurement when the inlet liquid temperature is different to the inlet air temperature without any power dissipation at the semiconductor. In this constellation, the coupling thermal resistance R_{TH-WA} can be calculated from the power flow and temperature difference between liquid and air. In this case, it is assumed that only a negligible amount of the heat flows through the semiconductor (path through R_{TH-JA} and R_{TH-JW}). Estimating the thermal impedance to the junction of the semiconductor is more challenging, because the junction temperature is not available in general. Nevertheless, it is possible to estimate the inner power share according to Fig. 1b. This inner power share means that the primary power flows to the air ($P_{DUT\ Air}$) and to the liquid ($P_{DUT\ Water}$). These flows can be calculated by subtract/add the thermal flow through R_{TH-WA} ($P_{Water\ to\ Air}$). According to the thermodynamics, this

inner thermal share depends on the temperature difference between the water and air. Following this way it is possible to create a new model which only consists of one thermal coupling impedance between the water and air and an inner power share function depending on this difference. By applying various temperature differences (between water and air) this inner power share function can be estimated.

Using this approach, the thermal model is defined without the need for estimating or measuring the junction temperature. Finally the thermal impedance R_{TH-JW} has to be estimated. This is done by calculating the thermal share from manufacturing data for the healthy state. In the same way it can be calculated which R_{TH-JW} results for the actual health state.

3 Experimental Validation

An down-scaled experimental setup has been constructed to validate the proposed condition monitoring principle as shown in Fig. 2. The setup also incorporates a fan that is used for forced air cooling. With a heat exchanger the cooling water is conditioned to a desired temperature and flow. Different temperature sensors and a flow meter are connected to a data-logger.

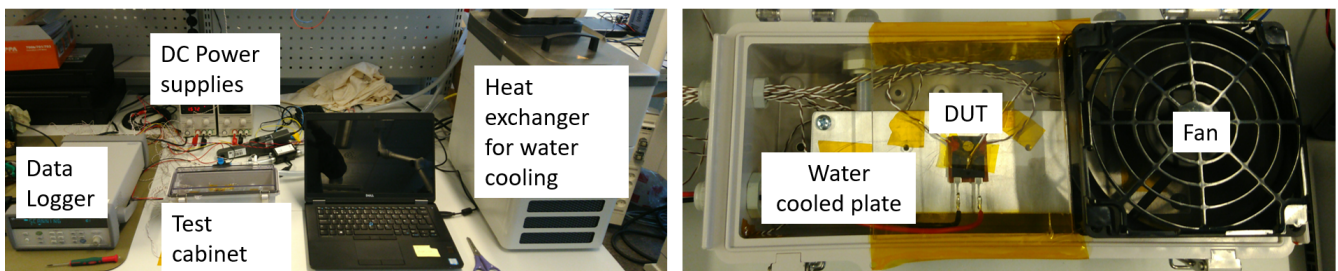


Fig. 2: Laboratory build-up for thermal monitoring

For the first set of measurements the devices under test (DUTs) are resistors encapsulated in TO-247 package. The increased thermal impedance is realised by applying several thermal pads under the case. The system is running until all temperatures reach steady state and the data logger is started. Now the power is turned on and run until a thermal steady state is reached again.

The results of a simple test are presented in Fig. 3. The image on the left shows the situation without powering on the DUT. Because the cooling water has higher temperature than the air, a power flow of 6W from the water to the air is measured. This is the power that has to be added/subtracted to estimate the inner power share. The image in the middle shows the power share when the DUT is mounted with 4 thermal pads. In brackets the inner power share is noted. Finally, the right image shows the anticipated power share when the DUT is mounted with 5 thermal pads (increased impedance). Based on these experiments, it is revealed that the proposed principle works well.

Experimental results using cycled SiC MOSFETs exhibiting a larger thermal impedance will be shown in the full paper and compared to healthy devices. Moreover, the estimation accuracy and a sensitivity analysis of the proposed method will be analysed in the final paper.

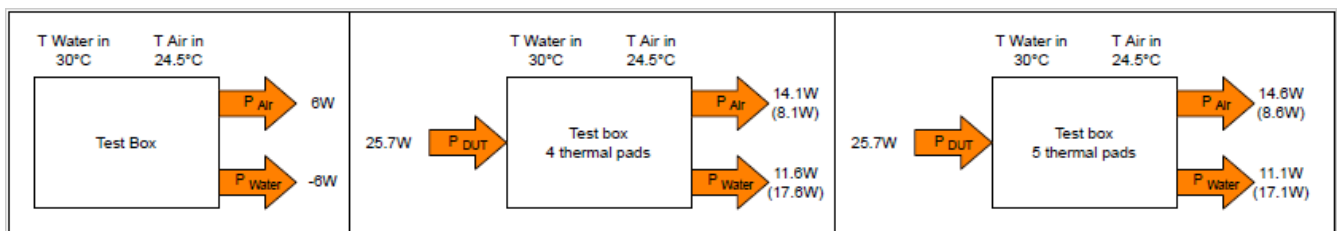


Fig. 3: Results from the build-up with the resistor and thermal pads

References

- [1] S. Peyghami, Z. Wang, and F. Blaabjerg, "A Guideline for Reliability Prediction in Power Electronic Converters," en, *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10 958–10 968, Oct. 2020. DOI: 10.1109/TPEL.2020.2981933.
- [2] E. R. Motto and J. F. Donlon, "IGBT module with user accessible on-chip current and temperature sensors," en, in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, USA: IEEE, Feb. 2012, pp. 176–181. DOI: 10.1109/APEC.2012.6165816.
- [3] N. Baker, F. Iannuzzo, S. Beczkowski, and P. K. Kristensen, "Proof-of-Concept for a Kelvin-Emitter On-Chip Temperature Sensor for Power Semiconductors," en, in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Genova, Italy: IEEE, Sep. 2019, P.1–P.8. DOI: 10.23919/EPE.2019.8914963.
- [4] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Junction temperature measurements via thermo-sensitive electrical parameters and their application to condition monitoring and active thermal control of power converters," en, in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Vienna, Austria: IEEE, Nov. 2013, pp. 942–948. DOI: 10.1109/IECON.2013.6699260.
- [5] F. Yang, E. Ugur, and B. Akin, "Evaluation of Aging's Effect on Temperature-Sensitive Electrical Parameters in SiC mosfets," en, *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6315–6331, Jun. 2020. DOI: 10.1109/TPEL.2019.2950311.
- [6] Z. Hu, M. Du, and K. Wei, "Online Calculation of the Increase in Thermal Resistance Caused by Solder Fatigue for IGBT Modules," en, *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 4, pp. 785–794, Dec. 2017. DOI: 10.1109/TDMR.2017.2746571.